IN THE CLAIMS

Claims 18-21, 27-31, and 33 are pending in this application. Please cancel claims 11-17, 25, 26, and 32 without prejudice or disclaimer as follows:

1-17. (Cancelled)

18. (Previously Presented) A non-volatile memory element comprising:

an SiC surface structure;

a floating-gate structure formed on said SiC surface structure, wherein said floating-gate structure includes an interface control layer, a first insulator barrier layer, a floating-gate layer formed of a metal or a semiconductor quantum well, a second insulator barrier layer, and a gate electrode layer, wherein said interface control layer is a Group-III nitride layer formed in contact with said SiC surface structure and having a film thickness in the range of one molecule-layer to a critical film thickness such that no misfit dislocation occurs with said SiC surface structure; and

a source and a drain formed on said SiC surface structure adjacent to said floating-gate structure.

19. (Previously Presented) The nonvolatile memory element according to claim 18, wherein said interface control layer is AlN having a thickness of 6 nm or smaller.

20. (Previously Presented) The field effect transistor according to claim 18, wherein said first insulator barrier layer has a double-layered film structure on said interface control layer, said double-layered film structure comprising an Al_2O_3 layer and a SiO_2 layer layered in order.

21. (Previously Presented) The nonvolatile memory element according to claim 18, wherein said first insulator barrier layer comprises a layer formed from a material that is different from said interface control layer and that has a greater band offset with respect to a conduction carrier than said interface control layer.

22. (Withdrawn) A method for manufacturing a field effect transistor comprising the steps of:

preparing a substrate having a SiC surface structure;

forming a source and a drain in said SiC surface structure;

controlling a step structure on the surface of said SiC surface structure and cleaning said surface;

forming an interface control layer adjacent to said SiC surface structure by layer-by-layer growth or step-flow growth, wherein said interface control layer is a Group-III nitride layer and has a thickness of one molecule-layer or greater to a critical film thickness such that no misfit dislocation occurs with said SiC surface structure;

forming an insulating layer on said interface control layer from a material different from that of said interface control layer and having a greater band offset with respect to a conduction carrier than said interface control layer ; and

forming a gate electrode on said insulator layer.

23. (Withdrawn) The method for manufacturing a field effect transistor according to claim 22, wherein said Group-III nitride layer comprises AlN and has a thickness of 6 nm or smaller.

24. (Withdrawn) The method for manufacturing a field effect transistor according to claim 11, wherein said SiC surface structure comprises a plane having an offset angle of 15 degrees or smaller with respect to the (0001) plane of 4H-SiC or 6H-SiC, wherein, for controlling the step structure, a step-terrace structure having a height corresponding to the unit period (c-axis lattice constant) of each SiC.

25-26. (Canceled)

27. (Previously Presented) A nonvolatile memory element comprising:

an SiC surface structure;

a floating-gate structure formed on said SiC surface structure including a first insulator barrier layer, a well layer, a second insulator barrier layer, and a gate electrode layer, wherein said first insulator barrier layer is formed in contact with said SiC surface structure and comprises a Group-III nitride epitaxial layer, said well layer is formed of a Group-III nitride epitaxial layer and functions as a floating gate, and said second insulator barrier layer is formed of a Group-III nitride epitaxial layer; and

a source and a drain formed in said SiC surface structure adjacent to said floating-gate structure.

28. (Previously Presented) The nonvolatile memory element according to claim 27, wherein said first insulator barrier layer is a Group-III nitride layer that has a film thickness in the range of one molecule-layer to a critical film thickness such that no misfit dislocation with said SiC surface structure occurs.

29. (Previously Presented) The nonvolatile memory element according to claim 27, wherein said first insulator barrier layer is a layer comprised of AlN and having a thickness of one molecule-layer or greater to 6 nm or smaller.

30. (Previously Presented) The nonvolatile memory element according to claim 27, wherein said well layer contains Ga and N.

31. (Previously Presented) The nonvolatile memory element according to claim 27, wherein said second insulator barrier layer contains Al and N.

32. (Canceled)

33. (Previously Presented) The field effect transistor according to claim 19, wherein said first insulator barrier layer has a double-layered film structure on said interface control layer, said double-layered film structure comprising an Al_2O_3 layer and a SiO_2 layer layered in order.